IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Canceled).

Claim 2 (Currently Amended): ~~The micro-controller unit according to claim 1,~~ A micro controller unit comprising:

a clock generating circuit for generating first and second clocks having equal phases to each other;

a CPU (central processing unit) to be operated based on said first clock;

a peripheral device controlled by said CPU and operated based on said second clock;

a first bus to be operated based on said first clock;

a second bus to be operated based on said second clock; and

a BIU (bus interface unit) for controlling operation timings of said first and second buses,

wherein said clock generating circuit includes a register for holding setting of frequencies of said first and second clocks to be equal to each other or different from each other, and switches said frequencies of said first and second clocks depending on said setting held in said register with said phases of said first and second clocks maintained to be equal to each other,

said first and second clocks are input to said BIU,

said BIU alternately switches idle periods of said first and second buses at predetermined timings which are synchronous with said first and second clocks, thereby carrying out said operation timing control,

wherein said clock generating circuit further has a clock stop device which is controlled by said CPU to stop generation of said first and second clocks, and

said clock stop device stopping said generation of said first and second clocks synchronously with such a timing that a unit cycle in said second clock ends.

Claim 3 (Currently Amended): ~~The micro controller unit according to claim 1,~~ A micro controller unit comprising:

a clock generating circuit for generating first and second clocks having equal phases to each other;

a CPU (central processing unit) to be operated based on said first clock;

a peripheral device controlled by said CPU and operated based on said second clock;

a first bus to be operated based on said first clock;

a second bus to be operated based on said second clock; and

a BIU (bus interface unit) for controlling operation timings of said first and second buses,

wherein said clock generating circuit includes a register for holding setting of frequencies of said first and second clocks to be equal to each other or different from each other, and switches said frequencies of said first and second clocks depending on said setting held in said register with said phases of said first and second clocks maintained to be equal to each other,

said first and second clocks are input to said BIU,

said BIU alternately switches idle periods of said first and second buses at predetermined timings which are synchronous with said first and second clocks, thereby carrying out said operation timing control, and

wherein said clock generating circuit further includes means for setting said frequencies of said first and second clocks to be equal to each other irrespective of said setting held in said register.

Claim 4 (Currently Amended): ~~The micro-controller unit according to claim 1,~~ A micro controller unit comprising:

a clock generating circuit for generating first and second clocks having equal phases to each other;

a CPU (central processing unit) to be operated based on said first clock;

a peripheral device controlled by said CPU and operated based on said second clock;

a first bus to be operated based on said first clock;

a second bus to be operated based on said second clock; and

a BIU (bus interface unit) for controlling operation timings of said first and second buses,

wherein said clock generating circuit includes a register for holding setting of frequencies of said first and second clocks to be equal to each other or different from each other, and switches said frequencies of said first and second clocks depending on said setting held in said register with said phases of said first and second clocks maintained to be equal to each other,

said first and second clocks are input to said BIU,

said BIU alternately switches idle periods of said first and second buses at predetermined timings which are synchronous with said first and second clocks, thereby carrying out said operation timing control,

wherein said clock generating circuit generates said first and second clocks based on a predetermined reference clock, and further includes:

an oscillator for outputting a third clock;

a reference clock switching circuit for switching said reference clock into a predetermined external clock input from an outside of said clock generating circuit or said third clock; and

an external clock stop detecting circuit for monitoring said external clock, thereby detecting a stop of said external clock, and

said reference clock switching circuit switching said reference clock into said third clock when said stop of said external clock is detected.

Claim 5 (Currently Amended): ~~The micro-controller unit according to claim 4,~~ A micro controller unit comprising:

a clock generating circuit for generating first and second clocks having equal phases to each other;

a CPU (central processing unit) to be operated based on said first clock;

a peripheral device controlled by said CPU and operated based on said second clock;

a first bus to be operated based on said first clock;

a second bus to be operated based on said second clock; and

a BIU (bus interface unit) for controlling operation timings of said first and second buses,

wherein said clock generating circuit includes a register for holding setting of frequencies of said first and second clocks to be equal to each other or different from each other, and switches said frequencies of said first and second clocks depending on said setting held in said register with said phases of said first and second clocks maintained to be equal to each other,

said first and second clocks are input to said BIU,

said BIU alternately switches idle periods of said first and second buses at predetermined timings which are synchronous with said first and second clocks, thereby carrying out said operation timing control,

wherein said clock generating circuit generates said first and second clocks based on a predetermined reference clock, and further includes:

an oscillator for outputting a third clock;

a reference clock switching circuit for switching said reference clock into a predetermined external clock input from an outside of said clock generating circuit or said third clock; and

an external clock stop detecting circuit for monitoring said external clock, thereby detecting a stop of said external clock,

said reference clock switching circuit switching said reference clock into said third clock when said stop of said external clock is detected, and

wherein said clock generating circuit sets said frequencies of said first and second clocks to be equal to each other irrespective of said setting held in said register when said stop of said external clock is detected.